HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS COMPOSITE DATA SHEET

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

0°C TO 75°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild High Level Logic Diode-Transistor Micrologic® Integrated Circuit family (HLLDTμL) consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. Noise Immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of CCSL.

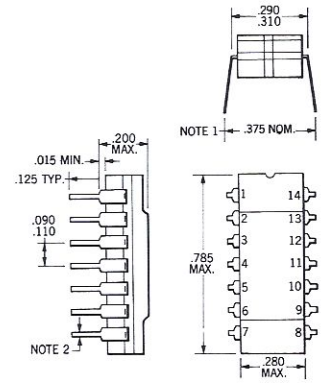
Interfacing from CCSL to HLLDTμL is accomplished with the 9112, shifting from HLLDTμL to CCSL is accomplished with the 9109. The 9112 can also be used to drive the μM3700 MOS Multiplexer.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar* and Epitaxial processes.

HLLDTμL elements are available in the hermetically sealed ceramic Dual In-Line Package (DIP), designed for automated and low cost insertion techniques.

TYPICAL DUAL IN-LINE PACKAGE

similar to
JEDEC (TO-116) Outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

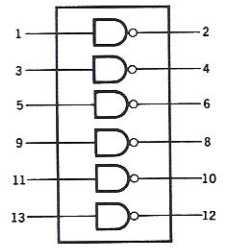
FEATURES

- **High Voltage Operation . . . V_{CC} Range 12 to 20 V.**
- **Utilizes inexpensive external input diodes to facilitate a high density building block approach and very high Logic Fan-In where desired.**
- **High D.C. Noise Immunity . . . 6.5 V minimum**
- **High A.C. Noise Immunity . . . 10 V at** 150 **ns**
- **Interfaces with CCSL**

ABSOLUTE MAXIMUM RATINGS (above which the reliability of the device may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
V_{CC} Pin Potential to Gnd Pin	−0.5 V to +25 V
Output Current when output is low	40 mA
Input Current (9109, 9110)	10 mA
Output Voltage	25 V
Input Voltage (9112)	5.5 V

LOGIC DIAGRAM



VCC = Pin 14
GND = Pin 7

ORDERING INFORMATION

To order HLLDTμL elements specify U6AXXXX59X, where XXXX is the four-digit number denoting the specific element desired.

*Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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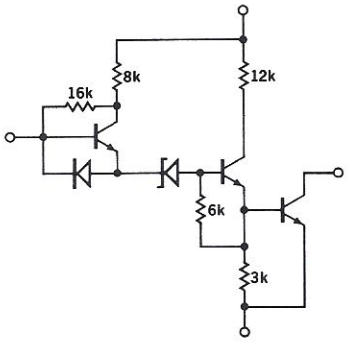
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	DEVICE	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	9110 9112	Note 2		Note 2			Note 2		Volts	V_{CC} = 12 V to 20 V I_{OH} = −0.1 mA @ V_{IL}
I_{CEX}I	Output Leakage Current	9109		75		1.0	75		75	μA	V_{CC} = 20 V V_{OH} = 20 V @ V_{IL}
V_{OL1}	Output Low Voltage	9109 9110 9112		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V I_{OL} = 10 mA @ V_{IH}
V_{OL2}	Output Low Voltage	9109 9110 9112		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V I_{OL} = 20 mA @ V_{IH}
V_{IL}	Input Low Voltage	9109 9110		7.05			7.0		6.8	Volts	Input Low Threshold @ V_{OH}
		9112		1.05			1.0		0.8		
V_{IH}	Input High Voltage	9109 9110	8.6		8.5			8.4		Volts	Input High Threshold @ V_{OL}
		9112	2.1		2.0			1.9			
I_F	Input Load Current	9109 9110 9112		−1.20		−0.80	−1.12		−1.12	mA	V_{CC} = 20 V, V_F = 0.5 V
I_{SC}	Output Short Circuit Current	9110 9112		−17 −2.4		−9.0 −1.65	−16.3 −2.3		−15.6 −2.3	mA	V_{CC} = 20 V, V_{IN} = 0 V V_{OUT} = 0 V
I_{CEX}	Output Leakage Current	9110 9112		75		1.0	75		75	μA	V_{CC} = 20 V, V_{OUT} = 20 V V_{IN} = 0 V
I_{PDH}	Input High Supply Current	9109 9110				19	28			mA	V_{CC} = 20 V, Input Open
		9112				22	34				
I_R	Input Leakage Current	9112					5.0		10	μA	V_{CC} = 20 V, V_R = 4.0 V
I_{max}	Ground Current	9109 9110 9112					15			mA	V_{CC} = V_{OUT} = 25 V, Inputs @ GND
t_{pd+}	Turn Off Delay	9109 9110 9112				145	300			ns	See Fig. 4
t_{pd-}	Turn On Delay	9109 9110				95	200			ns	See Fig. 4
		9112				30	125				
V_{TN}	"0" Level A.C. Noise Immunity	9110				7.0				Volts	See Fig. 5
V_{TP}	"1" Level A.C. Noise Immunity	9110				8.5				Volts	See Fig. 5

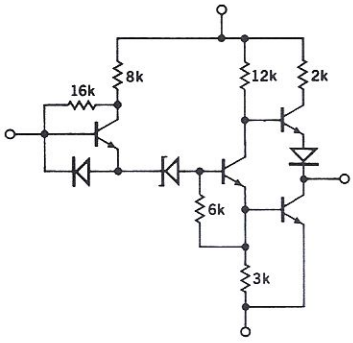
NOTES:
(1) Tests on 9109, 9110 are performed with FDH6 input diodes.
(2) MIN = Vcc −2.0 V for all temperature
TYP = Vcc −1.5 V for 25°C

Fig. 1a



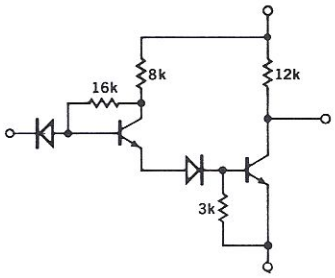
1/6 HLLDTL 9109
HLL → CCSL

Fig. 1b



1/6 HLLDTL 9110
HLL → HLL

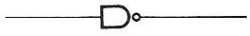
Fig. 1c



1/6 HLLDTL 9112
CCSL → HLL

Fig. 2a

$$\frac{1^*}{\text{LOW LEVEL LOAD FACTOR}}$$
(see Fig. 3a)



$$\frac{\text{9109: OPEN COLLECTOR}\quad \text{9110,9112: 20}}{\text{LOW LEVEL DRIVE FACTOR}}$$
(see Fig. 2b)

* WITH FDH6 INPUT DIODE FOR 9109,9110

Fig. 2b
OUTPUT LOADS
(LOW LEVEL DRIVE FACTOR)
VERSUS SUPPLY VOLTAGE

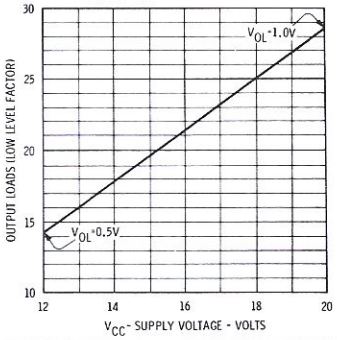


Fig. 3a
WORST CASE INPUT FORWARD
CURRENT AND INPUT LOADS
VERSUS SUPPLY VOLTAGE

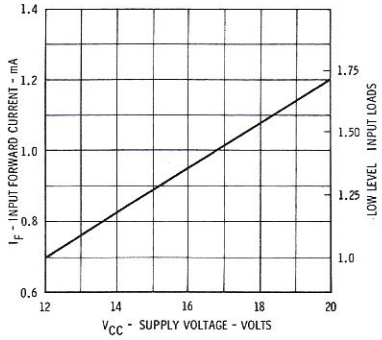


Fig. 3b
WORST CASE POWER DISSIPATION
VERSUS SUPPLY VOLTAGE
(PER GATE)

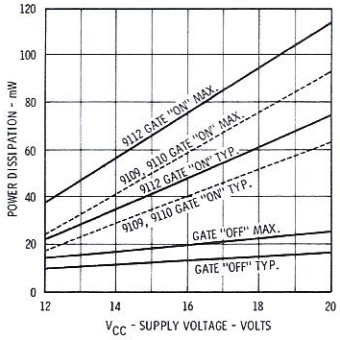


Fig. 3c
WORST CASE HIGH LEVEL
D.C. NOISE IMMUNITY
VERSUS TEMPERATURE

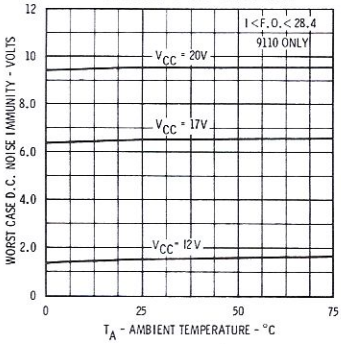


Fig. 3d
WORST CASE HIGH INPUT
THRESHOLD VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

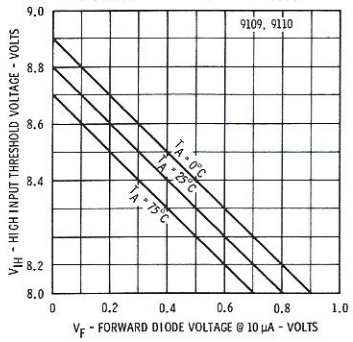


Fig. 3e
WORST CASE LOW THRESHOLD
VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

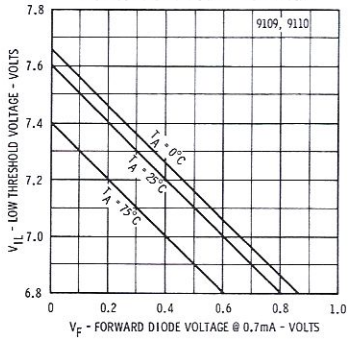


Fig. 3f
WORST CASE LOW LEVEL
D.C. NOISE IMMUNITY
VERSUS AMBIENT TEMPERATURE

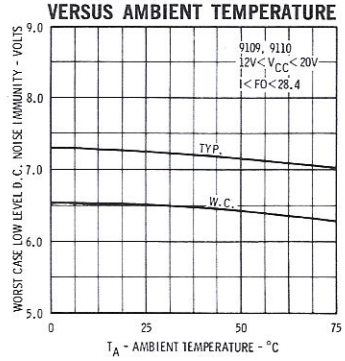


Fig. 3g
TURN OFF DELAY
VERSUS AMBIENT TEMPERATURE

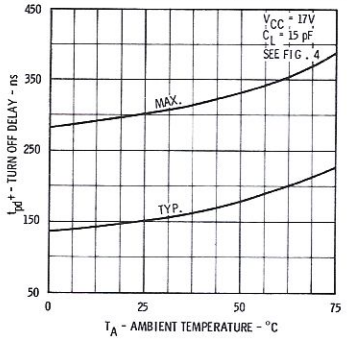


Fig. 3h
TURN ON DELAY
VERSUS AMBIENT TEMPERATURE

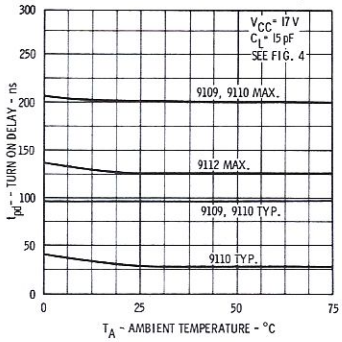


Fig. 3i
TYPICAL A.C. NOISE IMMUNITY
INPUT VOLTAGE VERSUS
PULSE WIDTH

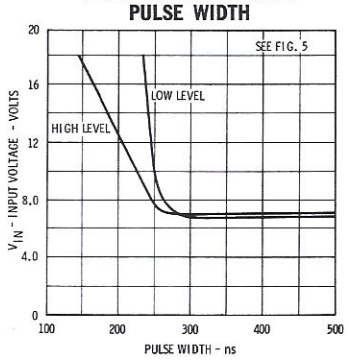
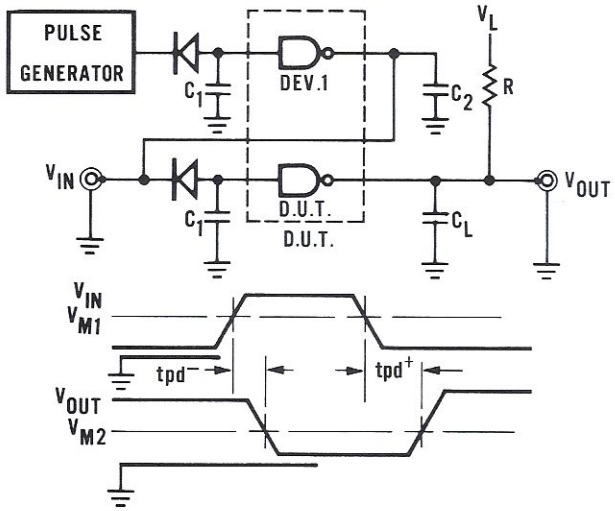


Fig. 4
SWITCHING TIME TEST CIRCUIT
AND WAVEFORMS



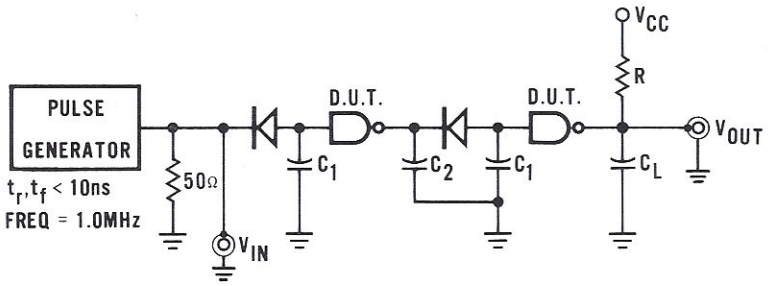
$C_1 = 5.0$ pF Includes all probe
$C_2 = 10$ pF and jig capacitance
$C_L = 15$ pF

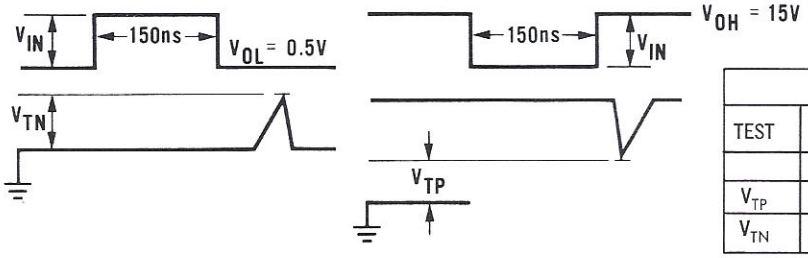
FDH6 Input Diodes are
used on 9109, 9110

TEST CONDITIONS

D.U.T.	DEV. 1	V_{m1}(V)	V_{m2}(V)	V_L(V)	R_{tpd-}	R_{tpd+}
9109	9110	7.5	1.5	5.0	510 Ω	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k

Fig. 5
A.C. NOISE IMMUNITY TEST CIRCUIT



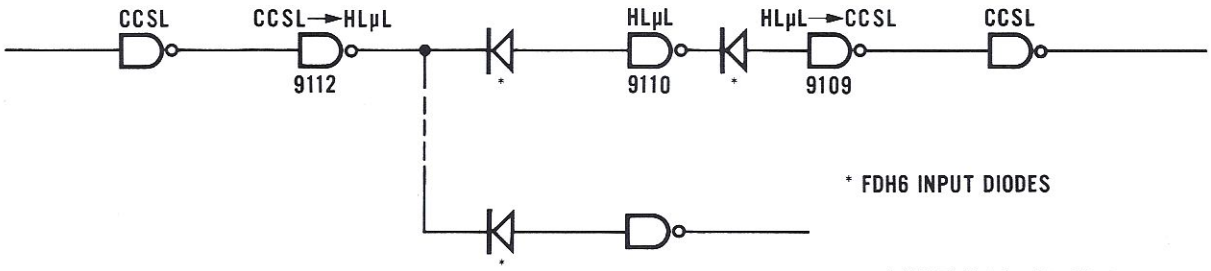


Unused inputs grounded
diodes are FDH6
$C_1 = 5.0$ pF Includes jig and
$C_2 = 10$ pF all probe capacitance
$C_L = 15$ pF

TEST CONDITIONS AND LIMITS						
TEST	LIMIT		V_{CC}	R	T_A	V_{IN}
	MIN.	MAX.	(Volts)	(kΩ)	(°C)	(Volts)
V_{TP}	8.5 V		17	24	25	10
V_{TN}		7.0 V	17	2.4	25	10

APPLICATIONS:

Fig. 6—CCSL INTERFACING



1 HLLDTL High Level Load Factor
= 1 CCSL High Level Load Factor
1 HLLDTL Low Level Load Factor
= 7.5 CCSL Low Level Load Factors

Fig. 7—LAMP DRIVER

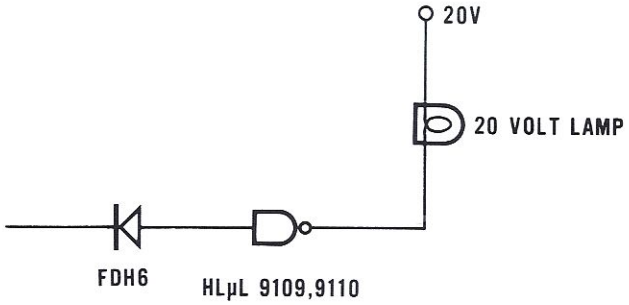
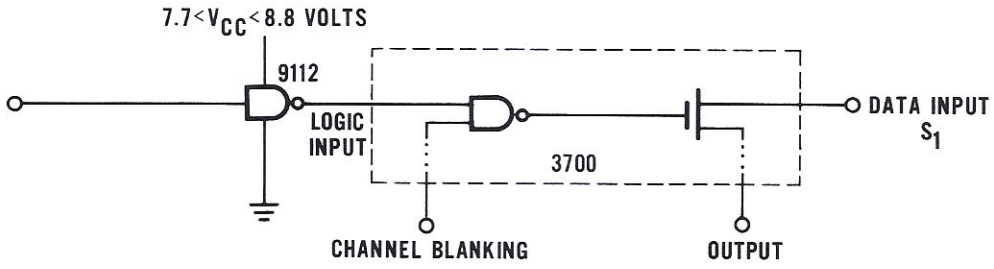
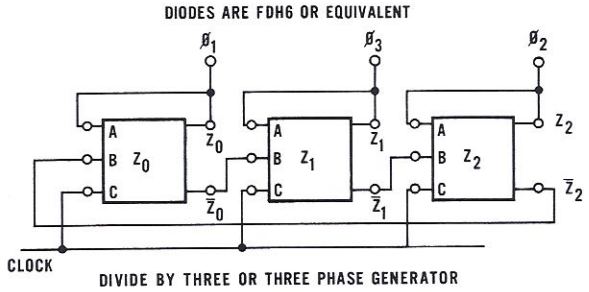


FIG. 8—DRIVING MOS3700 MULTIPLEXER OR EQUIVALENT



Output Levels : min "1" level = V_{CC} —1.5 V
: max "0" level = 0.2 V

Fig. 9—SEQUENTIAL COUNTER



ϕ_1	ϕ_3	ϕ_2	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

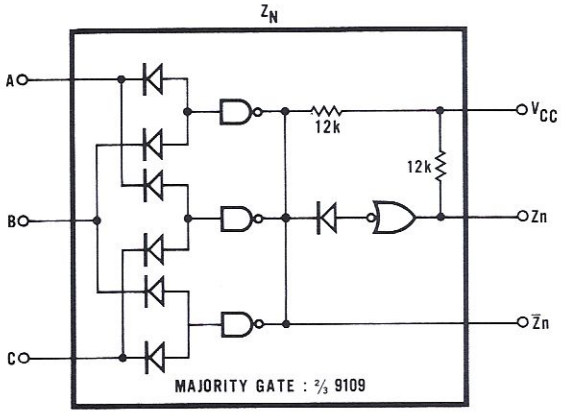
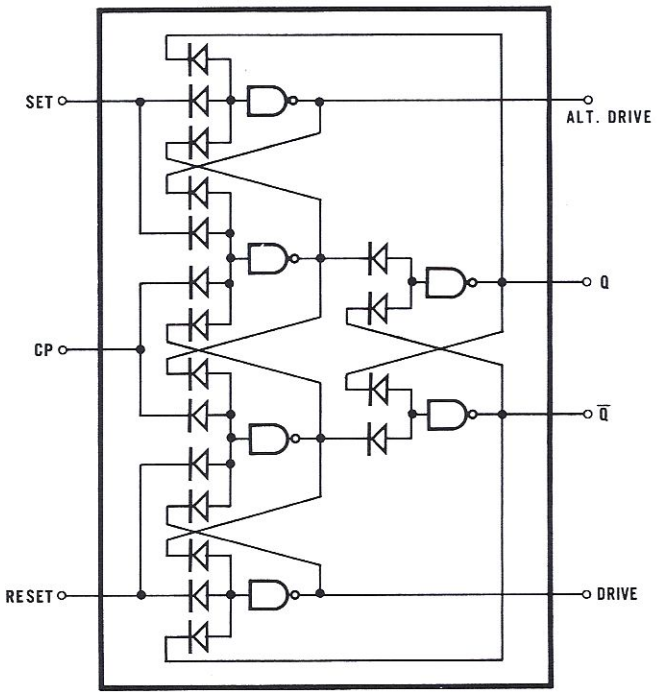
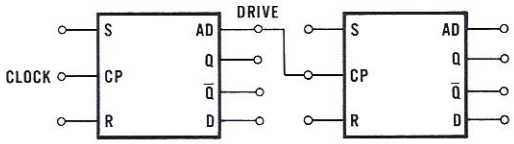
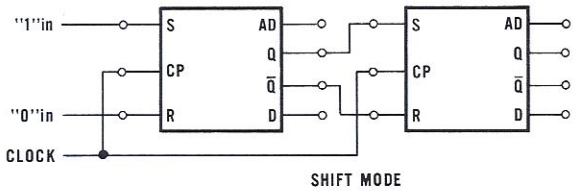


Fig. 10—JK FLIP FLOP







DIODES ARE FDH6 OR EQUIVALENT

J	K	Qn+1
L	H	L
L	L	Qn
H	H	$\overline{Q}$n
H	L	H

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